SEMICONDUCTOR DEVICE

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor device.

BACKGROUND ART

[0002] In general, semiconductor devices are classified into lateral semiconductor devices, wherein electrodes are formed on one surface of a semiconductor substrate, and vertical semiconductor devices, which have electrodes on both surfaces of a semiconductor substrate. In the vertical semiconductor device, a direction in which a drift current flows in an on-state, and a direction in which a depletion layer caused by a reverse bias voltage extends in an off-state, are the same. In a conventional planar n-channel vertical MOSFET (MOSFET: metal oxide semiconductor field effect transistor), a high resistivity n^- drift layer works as a region that makes a drift current flow in the vertical direction in the on-state. Consequently, as the drift resistance is reduced by shortening the current path of the n^- drift layer, an advantage lowering the on-resistance of the MOSFET is obtained.

[0003] Meanwhile, the high resistivity n^- drift layer is depleted in an off-state in order to increase a breakdown voltage. Therefore, when the n^- drift layer becomes thinner, the width of a drain-to-base depletion layer spreading from a p-n junction between a p-base region and the n^- drift layer becomes smaller, and the breakdown voltage decreases. Conversely, as the n^- drift layer is thick in a semiconductor device with high breakdown voltage, the on-resistance increases and the conduction loss increases. In this way, there is a trade-off relationship between on-resistance and breakdown voltage.

[0004] It is known that this trade-off relationship is also established in the same way in a semiconductor device such as an IGBT (insulated gate bipolar transistor), bipolar transistor, or diode. Also, the trade-off relationship is also the same in a lateral semiconductor device, wherein a direction in which a drift current flows in the on-state, and a direction in which a depletion layer caused by a reverse bias extends in the off-state, are different.

[0005] In the specification and attached drawings, a layer or region being prefixed by n or p means that a large number of electrons or positive holes respectively are carriers. Also, + or − appended to n or p means that there is a higher impurity concentration or lower impurity concentration than in a layer or region to which + or − is not appended.

[0006] FIG. **39** is a sectional view showing a heretofore known superjunction semiconductor device. As a method of solving, the problem caused by the heretofore described trade-off relationship, a superjunction (SJ) semiconductor device is commonly known, wherein the drift layer is a parallel p-n layer **120** with an n-type region **101**, with an increased impurity concentration, and a p-type region **102** are repeatedly alternately joined. A p-base region **103**, an n-type surface region **104**, a p contact region **105**, an n source region **106**, a gate insulating film **107**, a gate electrode **108**, an interlayer insulating film **109**, and a source electrode **110** are provided as a surface structure in an active portion. A drain electrode **112** in contact with an n^+ drain region **111** is provided on a second main surface (for example, refer to Patent Document 1, Patent Document 2, and Patent Document 3). The parallel p-n layer **120** is provided between the surface structure and the n^+ drain region **111**.

[0007] FIG. **40** is a diagram showing impurity concentration. distributions of the superjunction semiconductor device shown in FIG. **39**. FIG. **40** shows an n-type impurity concentration distribution (along a cut line AA-AA') in the second main surface side direction (hereafter referred to as the depth direction) from an end portion (hereafter referred to as the upper end) on the first main surface side of the n-type surface region **104**, and a p-type impurity concentration distribution (along a cut line of BR-RW) in the depth direction from the upper end of the p^+ contact region **105**. A first depth d_0 is the depth from the upper end of the p-base region **103** to an end portion (hereafter referred to as the lower end) on the second main surface side of the p-base region **103**. A second depth d_{10} is the depth from the lower end of the p-base region **103** to the lower end of the p-type region **102**. In FIG. **39**, the impurity concentrations of the n-type region **101** and p-type region **102** are even in the depth direction.

[0008] In a semiconductor device with this kind of structure, as a depletion layer spreads in a lateral direction from each p-n junction extending in the vertical direction of the parallel p-n layer when in an off-state, depleting the whole drift layer, even when the impurity concentration of the parallel p-n layer is high, it is possible to achieve a high breakdown voltage.

[0009] Also, the following kind of device is proposed as another superjunction semiconductor device that achieves an improvement in breakdown voltage and a reduction in on-resistance. The device has a superjunction structure formed by cyclically and alternately disposing a first n-type pillar layer, a p-type pillar layer, and a second n-type pillar layer on an n^+ type drain layer. The p-type pillar layer and second n-type pillar layer are such that the impurity concentration on a source electrode side is higher than that on a drain electrode side (for example, refer to Patent Document 4).

[0010] Also, as another device, the following kind of device is proposed. The device has a first conductivity type first semiconductor pillar layer formed on a main surface of a first conductivity. type first semiconductor substrate, a second conductivity type second semiconductor pillar layer adjacent to the first semiconductor pillar layer, a first conductivity type third semiconductor pillar layer adjacent to the second semiconductor pillar layer, and a second conductivity type semiconductor base layer provided on an upper surface of the second semiconductor pillar layer, and a MOS transistor is formed on the semiconductor base layer. The carrier concentration in an upper side region of the first to third semiconductor pillar layers is set to be higher than the carrier concentration in a lower side region (for example, refer to Patent Document 5).

[0011] Also, as another device, the following kind of device is proposed. There is a parallel p-n structure portion wherein an n-type drift region and a p-type partition region are alternately disposed on an n^+ drain region, a p-base region is formed on the p-type partition region, and an n^+ source region and p^+ contact region are formed selectively on a surface layer of the p-base region. A surface n-type drift region with a high impurity concentration is formed above the n-type drift region. A gate electrode is provided across a gate insulating film on the front surface of a p-base region sandwiched by the surface n-type drift region and source region. A source electrode is provided in contact with the front surfaces of both the n^+ source region and p^+ contact region, and a drain electrode is provided in contact with the backside surface of the n^+ drain